CLAIMS

What is claimed is:

1. In a processor adapted to cooperate with a coprocessor coupled thereto via a communication bus in an execution of at least one instruction comprising a count field and a code field, a method for executing said instruction comprising the steps of:
receiving said instruction;
providing to said coprocessor, via a first cycle on said communication bus, said count and code fields;
if the count field has a value, n, greater than zero, providing to the coprocessor, via a second cycle on said communication bus, a first operand; and
completing said instruction.

2. The method of claim 1 wherein said instruction has a mnemonic of H_CALL.

3. The method of claim 1 further comprising the steps of:
receiving a first input signal from the coprocessor via said communication bus during said first cycle.

4. The method of claim 3 wherein, if the first input signal received from the coprocessor via the communication bus during said first cycle has a first state, then repeating said first cycle, wherein the step of repeating said first cycle includes:
providing to said coprocessor, via said first cycle on said communication bus, said count and code fields; and
receiving said first input signal from the coprocessor via said communication bus during said first cycle.

5. The method of claim 4 wherein, if the first input signal received from the coprocessor via the communication bus during said first cycle has a second state, then providing to said coprocessor, via said second cycle on said communication bus, a first output signal.

6. The method of claim 5 further characterized in that the first output signal is selectively provided to the coprocessor via said second cycle on said communication bus.

7. The method of claim 4 further comprising the steps of:
if a count field value, n, is greater than one, then, on each of (n-1) cycles on said communication bus:
providing to the coprocessor, via said communication bus, a next one of (n-1) operands; and
receiving from the coprocessor, via said communication bus, a second input signal.

8. The method of claim 7 wherein, if the second input signal received from the coprocessor via the communication bus during a cycle, m, of said (n-1) cycles, has a first state, then repeating said cycle m, wherein said step of repeating said cycle m includes:
providing to the coprocessor, via said communication bus, the operand m; and
receiving from the coprocessor, via said communication bus, said second input signal.

9. The method of claim 1 further comprising the steps of:
if a count field value, n, is greater than one, then, on each of (n-1) cycles on said communication bus:
providing to the coprocessor, via said communication bus, a next one of (n-1) operands; and
receiving from the coprocessor, via said communication bus, a second input signal.

10. The method of claim 9 wherein, if the second input signal received from the coprocessor via the communication bus during a cycle, m, of said (n-1) cycles, has a first state, then repeating said cycle m, wherein said step of repeating said cycle m includes:

providing to the coprocessor, via said communication bus, the operand m; and

receiving from the coprocessor, via said communication bus, said second input signal.

11. The method of claim 1 wherein the processor is adapted to cooperate with a plurality of coprocessors coupled thereto via said communication bus in the execution of said instruction, the method further comprising the step of:

providing to said plurality of coprocessors, via said communication bus during said first cycle, an identifier field having a value which uniquely identifies a selected one of said plurality of coprocessors.

12. The method of claim 1 wherein the processor includes a plurality of registers for storing selected operands, and wherein the step of providing said first operand to said coprocessor via said communication bus during said second cycle is further characterized as:

if the count field has a value, n, greater than zero, providing to the coprocessor, via a second cycle on said communication bus, an operand stored in a predetermined one of said plurality of registers.

13. The method of claim 1 further including the step of:

providing to the coprocessor, during at least a portion of said second cycle on said communication bus, a second output signal.

14. In a processor adapted to cooperate with a coprocessor coupled thereto via a communication bus in an execution of at least one instruction comprising an effective address calculation field, a method for executing said instruction comprising the steps of:

receiving said instruction;

providing to said coprocessor, via a first cycle on said communication bus, said effective address calculation field;

calculating an effective address in accordance with said effective address calculation field;

fetching an operand stored at said calculated effective address;

providing to the coprocessor, via a second cycle on said communication bus, said fetched operand; and

completing said instruction.

15. The method of claim 14 wherein said instruction has a mnemonic of H_LD.

16. The method of claim 14 further comprising the steps of:

receiving a first input signal from the coprocessor via said communication bus during said first cycle.

17. The method of claim 16 wherein, if the first input signal received from the coprocessor via the communication bus during said first cycle has a first state, then repeating said first cycle, wherein the step of repeating said first cycle includes:

providing to said coprocessor, via said first cycle on said communication bus, said effective address calculation field; and

receiving said first input signal from the coprocessor via said communication bus during said first cycle.

18. The method of claim 16 wherein, if the first input signal received from the coprocessor via the communication bus during said first cycle has a second state, then providing to said coprocessor, via said second cycle on said communication bus, a first output signal.

19. The method of claim 18 further characterized in that the first output signal is selectively provided to the coprocessor via said second cycle on said communication bus.

20. The method of claim 14 further including the step of:
providing to the coprocessor, during at least a portion of said second cycle on said communication bus, a first output signal.

21. The method of claim 14 wherein the processor includes a plurality of registers for storing selected operands, wherein the effective address calculation field comprises a base register designator subfield and a displacement subfield, and wherein the step of calculating said effective address in accordance with said effective address calculation field includes adding the contents of said displacement subfield to the contents of the one of said plurality of registers designated by the contents of said base register designator subfield.

22. The method of claim 21 wherein the effective address calculation field includes an update field and wherein the step of calculating said effective address in accordance with said effective address calculation field includes storing said calculated effective address in said designated one of said plurality of registers if said update field has a first value.

23. In a processor adapted to cooperate with a coprocessor coupled thereto via a communication bus in an execution of at least one instruction comprising an effective address calculation field, a method for executing said instruction comprising the steps of:

receiving said instruction;

providing to said coprocessor, via a first cycle on said communication bus, said effective address calculation field;

calculating an effective address in accordance with said effective address calculation field;

receiving from the coprocessor, via a second cycle on said communication bus, an operand;

storing said received operand at said calculated effective address; and

completing said instruction.

24. The method of claim 23 wherein said instruction has a mnemonic of H_ST.

25. The method of claim 23 further comprising the steps of:

receiving a first input signal from the coprocessor via said communication bus during said first cycle.

26. The method of claim 25 wherein, if the first input signal received from the coprocessor via the communication bus during said first cycle has a first state, then repeating said first cycle, wherein the step of repeating said first cycle includes:

providing to said coprocessor, via said first cycle on said communication bus, said effective address calculation field; and

receiving said first input signal from the coprocessor via said communication bus during said first cycle.

27. The method of claim 25 wherein, if the first input signal received from the coprocessor via the communication bus during said first cycle has a second state, then providing to said coprocessor, via said second cycle on said communication bus, a first output signal.

28. The method of claim 27 further characterized in that the first output signal is selectively provided to the coprocessor via said second cycle on said communication bus.

29. The method of claim 23 further including the step of:
receiving from the coprocessor, during at least a portion of said second cycle on said communication bus, a second input signal.

30. The method of claim 23 further including the step of:
providing to the coprocessor, during at least a portion of a third cycle on said communication bus, a first output signal.

31. The method of claim 23 wherein the processor includes a plurality of registers for storing selected operands, wherein the effective address calculation field comprises a base register designator subfield and a displacement subfield, and wherein the step of calculating said effective address in accordance with said effective address calculation field includes adding the contents of said displacement subfield to the contents of one of said plurality of registers designated by the contents of said base register designator subfield.

32. The method of claim 31 wherein the effective address calculation field includes an update field and wherein the step of calculating said effective address in accordance with said effective address calculation field includes storing said calculated effective address in said designated one of said plurality of registers if said update field has a first value.

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